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APPLICATION NOTE

Mounting consideration for SOT409 (ceramic SO-8) devices

AN98017





Application Note AN98017

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1 INTRODUCTION

For both 820 – 960 MHz (GSM) and 1800 – 1990 MHz (PCN and PCS), Philips has introduced a series of RF power transistors for base station applications at 26 V power supply. The driver stage transistors are mounted in a SO-8 style surface mount package (SOT409B), suitable for pick and place assembly. SOT409B packages have an AIN substrate to electrically isolate the flange from the leads. Table 1 summarizes the RF performance and thermal resistances of the transistors.

Table 1 SOT409B driver stage transistors with typical values between brackets

TRANSISTOR TYPE	f (MHz)	PL-1 dB (W)	Gp (dB)	Eff (%)	R _{thj-mb} (K/W)	P _{dmax} (W)
BLV904	960	5	>13 (15.5)	>50 (55)	10	17
BLV909	960	9	>9.5 (11.5)	>50 (55)	6	29
BLV2042	1990	4	>11 (13)	>40 (45)	10	17

In this paper the mounting of the SOT409B devices is considered. By focusing on the heatflow from junction (at die level) to the heatsink of the application, criteria for best thermal performance (lowest thermal resistance between mounting base and heatsink), can be derived. Simulation results are presented to show the behaviour of using different ways of mounting the device, resulting in a proposal for surface mounted assembly.

2 MOUNTING OF SOT409B DEVICES

Thermal investigations has shown that both the copper pad of the device's backside (connected to the AIN substrate) as well as the leads of the SOT409B, contribute to the heat transfer from junction to heat-sink. For the most optimal results two options are available:

The most effective way to thermally connect the SOT409B devices, is to directly solder the device's backside, together with the device's emitter leads (4 are available, at the edges; see Fig.1) to the heatsink or to an insert mounted to the heatsink; see Fig.2. A more practical option is a footprint on the P.C.B. with a number of through metallized holes to transfer the heat. In that case the device's copper pad is soldered to a footprint, of at least the same dimensions as the device (see Fig.3). Connection to the fully metallized backside of the P.C.B. is achieved by placing a sufficient number of plated through metallized holes just under the device:

- To achieve good grounding for best R.F. performance
- To optimize the heat transfer.

To optimize the thermal contact between the board and the heatsink a thin coating of thermal past should be applied locally to minimize voids. Further that P.C.B. should be fastened to the heatsink with extra screws as close as possible to the device. Another possibility is to solder the P.C.B. to the heatsink or use thermal conductive glue.

Pinning SOT409B

PIN	DESCRIPTION	
1	emitter	
2	base	
3	base	
4	emitter	
5	emitter	
6	collector	
7	collector	
8	emitter	

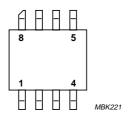
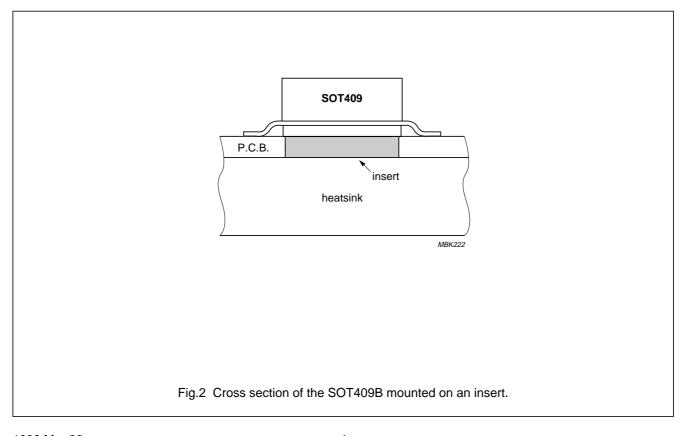
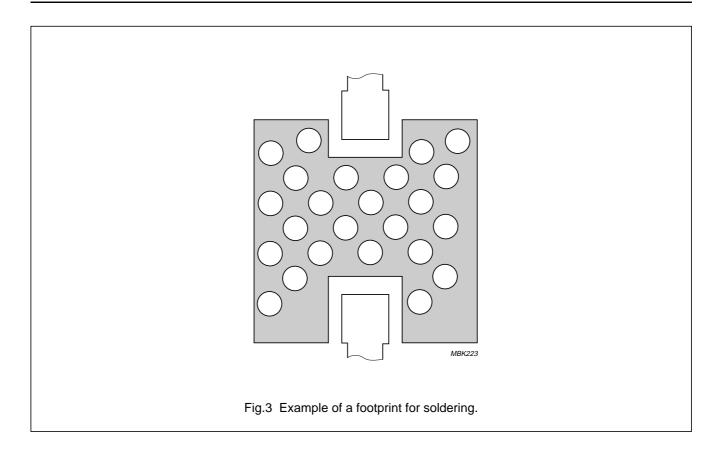


Fig.1 SOT409B outline.



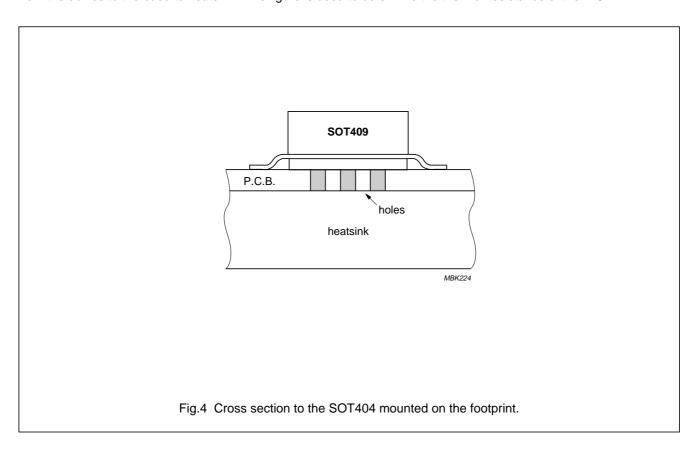
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3 HEATFLOW IN APPLICATION

In Fig.4 a cross section and a schematical representation is given of an application in which a mounted SOT409B device is used. The device has been mounted on top of a P.C.B. equipped with through metallized holes to transfer the heat from the device to the base to heatsink. This figure is used to determine the thermal resistance of the P.C.B.



4 IMPORTANT FACTORS FOR THERMAL RESISTANCE OF THE P.C.B.

- · Thickness of P.C.B. material
- Thickness of metallization of P.C.B.
- Copper growth in holes (depending on process used)
- Fill factor (percentage of solder present in through plated holes)
- Number of plated through holes
- Diameter of plated through holes.

Other parameters were taken into consideration, but have marginal effects on thermal resistance:

- P.C.B. material used (Duroid, epoxy)
- Pb percentage in PbSn.

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5 SIMULATION EXAMPLES

With the help of simulations, each of the critical factors have been investigated. For calculations, the following parameters have been used.

- Heat area dimensions: 4.13 × 3.18 mm
- PbSn thickness on top of P.C.B. metallization (24 μm)
- Pb % in PbSn (37%)
- Cu growth in via holes (32 μm)
- · P.C.B. material (Duroid)
- P.C.B. copper thickness (1 Oz. or 35 μm).

The result on thermal resistance is given in Table 2 and 3, for 9 and 12 through metallized holes respectively:

Table 2 Footprint area equipped with 9 through metallized holes

CASE	FILL FACTOR (%)	HOLES DIAMETER (mm)	P.C.B. THICKNESS (mm)	Rth mb-hs (K/W)
1	10	0.65	0.79	5.4
2	100	0.65	0.79	3.4
3	100	0.65	1.59	5.7
4	100	1.00	1.59	2.9
5	100	1.00	0.79	1.7

Table 3 Footprint area equipped with 12 through metallized holes

CASE	FILL FACTOR (%)	HOLES DIAMETER (mm)	P.C.B. THICKNESS (mm)	Rth mb-hs (K/W)	
1	10	0.65	0.79	_	
2	100	0.65	0.79	2.5	
3	100	0.65	1.59	4.3	
4	100	1.00	1.59	_	
5	100	1.00	0.79	1.3	

6 CONCLUSION

Using the material and permanent values given in the example, thermal resistance of the footprint design can be as low as 1.5 K/W for the optimum case. Even the most powerful transistor available in the SOT409B range, BLV909 (nominal 9 W of RF power at 960 MHz) can be operated with a sufficiently low junction temperature (T_j) . A T_j of 137 °C is possible while heatsink temperature (T_h) is assumed to be 70 °C and 50% collector efficiency is achieved at nominal loadpower.

7 REMARK

SOT409B is a SMD package which can withstand a normal reflow soldering process. Since the leads are plated with typically 3 μ m of gold, either sufficient solder material (\approx 150 μ m) should be applied or the leads should be pre-tinned in order to minimize brittle Au-Sn intermettalics which can introduce cracks during power cycling. A footprint for reflow soldering is available upon request.

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,

Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,

Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,

220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,

51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,

Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,

72 Tat Chee Avenue, Kowloon Tong, HONG KONG,

Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,

Tel. +45 32 88 2636, Fax. +45 31 57 0044 Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,

Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,

Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,

Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,

Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,

Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,

Tel. +82 2 709 1412, Fax. +82 2 709 1415 Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,

Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,

Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,

Tel. +64 9 849 4160, Fax. +64 9 849 7811 Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: UI. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain Romania: see Italy

Russia: Philips Russia, UI. Usatcheva 35A, 119048 MOSCOW,

Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,

Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,

2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,

Tel. +27 11 470 5911, Fax. +27 11 470 5494 South America: Al. Vicente Pinzon, 173, 6th floor,

04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22 08007 BARCELONA Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,

Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,

Tel. +41 1 488 2686, Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.

209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,

Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,

Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,

252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Haves. MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,

Tel. +1 800 234 7381

Uruguay: see South America Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,

Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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